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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/779,803	02/08/2001	Moinul I. Syed	A0312/7378 (RMA)	5583

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 07/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/779,803	SYED ET AL.	
	Examiner	Art Unit	
	Zhuo H. Li	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-6,30,32-36,39 and 41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-6,30,32-36,39 and 41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Stephen C. Elmore

STEPHEN C. ELMORE
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/15/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement filed on April 15, 2005 has been considered.

Response to Amendment

2. This Office action is in response to the amendment filed on April 15, 2005.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 6, 30, 34-36, 39 and 41 are rejected under 35 U.S.C. 102(e) as being anticipated by Hanawa et al. (US PAT. 6,282,505 hereinafter Hanawa).

Regarding claim 1, Hanawa discloses a cache memory system (430, figure 2) comprising a plurality of memory locations for storing data and addresses associated with the data wherein the memory locations are organized as two or more ways, i.e., data cache (430) comprising two memory banks (125 and 135, figure 2) wherein each of the memory is a cache memory of two-way set-association cache with respectively memory array (121-124 and 131-134, figure 2) and

(col. 5 line 55 through col. 6 line 44), at least one controller (160, figure 2) that enables a first device (100, figure 2) to access a first way selected from the two or more ways, i.e., memory array (121-124) in memory bank (125, figure 2) via the input selector (108, figure 2), and the output selector (146, figure 2) individually, and enables a second device (110, figure 2) to access a second way selected from the two or more ways, i.e., memory array (131-134) in the memory bank (135, figure 2) via the input selector (118, figure 2), and the output selector (156, figure 2) individually. In addition, Hanawa also teaches the first device can access a location in the first way and the second device is blocked from accessing the first way during access by the first device, wherein the second device can access a location in the second way and the first device is blocked from accessing the second way during access by the second device, i.e., memory bank (125) is capable access by the second device (110) via the address calculator (117, figure 1) and the address input selector (108), and memory bank (135) is also capable access by the first device (100) via the address calculator (107, figure 1) and the address input selector (118) individually (figure 3 and col. 7 line 23 through col. 8 line 56). Furthermore, Hanawa discloses the first and second ways can be accessing concurrently by the first and second devices, respectively (figure 2 and col. 7 lines 24-58 and col. 8 lines 30-45).

Regarding claim 6, Hanawa discloses a cache memory system (430, figure 2) comprising a plurality of memory locations for storing data and addresses associated with the data wherein the memory locations are organized as two or more ways, i.e., data cache (430) comprising two memory banks (125 and 135, figure 2) wherein each of the memory is a cache memory of two-way set-association cache with respectively memory array (121-124 and 131-134, figure 2) and (col. 5 line 55 through col. 6 line 44), a plurality of cache outputs (143 and 153, figure 2) for

providing data retrieved from the memory locations, and first and second multiplexers having multiplexer inputs (108 & 118, figure 2 and col. 5 line 55 through col. 6 line 6) coupled to at least some of the memory locations (bank 125 and bank 135, respectively), and multiplexer outputs (143,153, 146 and 156, figure 2) coupled to the plurality of cache outputs (col. 6 line 45 through col. 7 line 6), to enable a first multiplexer (108, figure 2) to access a first way selected from the two or more ways, i.e., memory array (121-124) in memory bank (125, figure 2) individually, and enables a second multiplexer (118, figure 2) to access a second way selected from the two or more ways, i.e., memory array (131-134) in the memory bank (135, figure 2) individually. In addition, Hanawa also teaches the first multiplexer can access a location in the first way and the second multiplexer can select data from a location in the second way, and the first and second ways can be accessing concurrently on respective ones of the plurality of cache outputs (figure 2 and col. 7 lines 24-58 and col. 8 lines 30-45).

Regarding claim 30, the limitation of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 34, the limitation of the claim are rejected as the same reasons set forth in claim 6.

Regarding claim 35, Hanawa teaches the method including an act of controlling first and second multiplexers to concurrently select as their respective outputs data from different ones of the first and second ways of the cache (col. 7 lines 23-58 and figure 2).

Regarding claim 36, the limitation of the claim are rejected as the same reasons set forth in claim 6.

Regarding claim 39, the limitation of the claim are rejected as the same reasons set forth in claim 35.

Regarding claim 41, the limitation of the claim are rejected as the same reasons set forth in claim 1.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 4-5 and 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanawa et al. (US PAT. 6,282,505 hereinafter Hanawa) in view of Liao et al. (US PAT. 6,857,061 hereinafter Liao).

Regarding claims 4-5, Hanawa discloses the cache system in a very long instruction word processor further comprising the first device includes a processor configured and arranged to access the memory locations (col. 5 lines 1-15). Hanawa differs from the claimed invention in not specifically teaching the second device includes a data transfer engine configured arranged to transfer data between the memory locations and a lower level memory, wherein the data transfer engine comprises a DMA controller. However, Liao teaches a microprocessor (10, figure 3) comprising control unit (18, figure 2), i.e., first device, level two cache (36, figure 3) with association tags array (38, figure 3), wherein the L2 cache is controlled by the control unit (18) and the bus interface unit/DMA (40, figure 3), i.e., second device, and further communicate with external memory (12, figure 3) (col. 6 lines 21-46 and col. 7 lines 31-56). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the super-scalar processor or a very long instruction word processor (VLIW processor) of Hanawa (col. 1 lines 7-11) in having a second device includes a data transfer engine configured arranged to transfer data between the memory locations and a lower level memory, wherein the data transfer engine comprises a DMA controller, as per teaching by the microprocessor of Liao, because Liao suggests the motivation for modifying Hanawa to incorporate the structure and functionality of Liao, which Liao provides an improved instruction format which may be used in connection with any suitable type of data processor, from microprocessor to supercomputers with a vector processing unit (col. 4 lines 33-37), thus, modifying Hanawa to incorporated the system of Liao would improve the vector processing system with a super-scalar processor or VLIW processor of Hanawa, and where it is inherent that super scalar processors an VLIW processor system perform data processing operations on vectors, furthermore, Liao further

suggested and noted such modification would result in improved vector operation processing (col. 6 lines 55-59), that is, improved operational efficiency for the combination of Hanawa in view of Liao.

Regarding claims 32-33, the limitation of the claims are rejected as the same reasons set forth in claims 4-5.

Response to Arguments

8. Applicant's arguments with respect to claims 1, 4-6, 30, 32-36, 39 and 41 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Jacobs (US PAT. 6,047,358) discloses computer system with cache memory and process for cache entry replacement with selective locking of elements in different ways and groups (abstract).

Yeager (US PAT. 6,594,728) discloses cache memory with dual-way arrays and multiplexed parallel output wherein the multiplexed outputs enable the cache memory to be more densely packed and implemented with fewer sense amplifiers (col. 2 lines 18-37).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 571-272-4183. The examiner can normally be reached on M-F 9:00am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li

Patent Examiner
Art Unit 2189

STEPHEN C. ELMORE
PRIMARY EXAMINER